REMARKS

Claims 1-14 are pending in this application.

Claims 3-7 and 11-12 stand rejected under 35 U.S.C. 112 as being indefinite

In addition, Claims 1 and 14 stand rejected under 35 U.S.C. 102(b) as being anticipated by Miller et al (hereinafter Miller) (US Patent 4, 368, 434).

In addition, Claims 8-9 and 12-13 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. in view of Alexander.

In addition, Claims 1-2 and 10 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Alexander in view of Davis.

The claims have been amended with a view of better defining the invention having regard to the Examiner's comments. Consequently, the Examiner is respectfully requested to consider the amended claims in view of the following comments.

Without limitation of the claims, the disclosed embodiments pertain to digital processing of data samples and to data path latency due to processing of samples through delay chains. Delay chains are introduced within digital systems to allow for various processing events, such as timing recovery of samples' boundaries. However, the processing of samples through such delay chains subsequent to the processing events that required them may unnecessarily add to the data path latency and, consequently, lead to suboptimal performance. Disclosed embodiments provide for reduction of the data path latency via reduction of the length of given delay chains. In particular, reduction of the length of a given delay chain is provided by eliminating delay elements from the delay chain, which is achieved by shifting samples out of the delay chain at an output rate higher than an input rate of reading additional samples into the delay chain.

Some of the disclosed embodiments provide further additional features for optimizing reduction of a delay chain consisting of pipelined registers such as bypassing empty registers. Performing a scaled reduction of the delay chain length in repeated phases is also disclosed.

Rejection of Claims 3-7 and 11-12 Under 35 U.S.C. § 112

The Examiner has rejected Claims 3, 7 and their dependent claims for making reference to the 802.11 industry standard. Accordingly, the claims have been amended to make reference

to the specific group of 802.11a, 802.11g and HIPERLAN/2 transmission systems, with support in the disclosure on page 3, lines 10-15.

Rejection of Claims 1 and 14 Under 35 U.S.C. § 102

The Examiner has rejected claims 1 and 14 as being anticipated by Miller et al. In view of the Examiner's comments and with a view to better defining the invention, independent Claims 1 and 14 have been amended to better define the invention.

In particular, claim 1 has been amended to specify "in response to receiving a signal of completion of a processing event, reducing the length of the delay chain by shifting samples rapidly out of the delay chain at a higher output rate than an input rate of samples coming into the delay chain". Support for this amendment can be found in the specification, such as on page 5, lines 13-17, page 9, lines 3-5.

In connection with former claim 1, the Examiner has contended that Miller et al. disclose the limitation of "subsequent to a processing event, shifting samples rapidly from the delay chain at a higher rate than samples coming "in col. 6, lines 24-26 and 42-46.

Applicant respectfully disagrees with the above. Miller et al. disclose a programmable discriminator 14 comprising programmable means for selecting the length of a delay line 20 and the rate at which samples are shifted through the line. The Applicant notes at least the following important facts distinguishing the above recitation of claim 1 from the Miller et al. disclosure.

Firstly, the Miller et al. programmable discriminator is intended for allowing demodulation of a variety of FSK signals, depending on the communication protocol being followed (col. 3, lines 39-47). The length of the Miller et al. delay line and the rate of shifting through the line are selected depending on the specific communication protocol being followed. The selection of these parameters is disclosed as being user (i.e. communication protocol or application) specific. In particular, the length of the delay line and the rate of moving through the line are changed in response to a DELAY SELECT and CLOCK SELECT control signals, respectively, which are provided by a Mode Control Read Only Memory (ROM) (col. 4, lines 19-26). The ROM contains, at various addresses, control signal values corresponding to a variety of applications (col. 4, lines 58-68). Given an FSK application, i.e. a mode, a certain length of the delay line can be selected. However, once the application or mode is defined, the read-only

memory card will only provide the application specific control signals, therefore the delay line length will be fixed for that application. This is in contrast to changes to the delay line length during operation of a specific application, in response to processing events. Applicant contends that Miller et al. do not disclose nor otherwise suggest reducing the length of the delay line subsequent to a processing event, or, as recited in amended claim 1, for further clarity, in response to receiving a signal completion of a processing event.

Secondly, Miller et al. indicate that the rate of shifting samples through the line can be varied, also depending on selected application. However, once an application is determined, the Miller et al. disclosure indicates a single rate of moving a signal through the line. Miller et al. do not disclose nor otherwise suggest a delay line provided with an output rate higher than an input rate. Therefore, Applicant indicates that Miller et al. do not teach "shifting samples rapidly out of the delay chain at a higher output rate than an input rate of samples coming into the delay chain".

Based on at least this reasoning, the Applicant believes that amended Claim 1 is not anticipated by Miller et al. The Applicant further contends that independent amended claim 14 reciting "means for reducing the length of the delay chain in response to receiving a signal of completion of a processing event", also patentably distinguishes over Miller et al. for at least the same reasons.

Rejection of Claims 8-9 and 12-13 Under 35 U.S.C. § 103

Claims 8, 9, 12 and 13 have been rejected by the Examiner as unpatentable over Miller et al., in combination with Alexander (US Patent 6, 765, 419 B2).

In particular, claim 8 has been amended to recite a "digital processing method" comprising "in response to receiving a signal of completion of synchronization of the data packet, reducing the length of the delay chain by shifting samples rapidly out of the delay chain at a higher output rate than an input rate of samples coming in to the delay chain". Support for this amendment can be found in the specification, such as on page 2, lines 23-27, page 5, lines 13-17, and page 9, lines 3-5.

In particular, the Examiner indicated that Miller et al. disclose a method of processing data samples comprising the step of "subsequent to synchronization of the data packet, shifting samples rapidly from the delay chain at a higher rate than samples coming in".

As previously argued with respect to claim 1, Applicant indicates that Miller et al. do not disclose nor otherwise suggest reducing the length of the delay line subsequent to synchronization of the data packet, or, as recited in amended claim 8, for further clarity, in response to receiving a signal of completion of synchronization of the data packet. Furthermore, Miller et al. do not teach "shifting samples rapidly out of the delay chain at a higher output rate than an input rate of samples coming into the delay chain".

Similarly, with respect to amended analogous system claim 8, Miller et al. do not teach nor otherwise suggest "a processor which controls the data shifting rates, the logic circuitry, and the output of the multiplexer based on a plurality of processing events of the apparatus".

Furthermore, the Examiner relied on Alexander for the disclosure of "reducing the length of the delay chain by bypassing empty registers". Applicant respectfully disagrees. Alexander discloses a delay lock loop comprising a forward delay circuit having a plurality of delay blocks, each of them including a plurality of units. The Applicant indicates that delay lock loops are analog processing circuits for processing clock signals as opposed to the digital detector of Miller et al. and to the claimed digital processing method of amended claim 8, for processing data samples, as claimed in amended claim 8. Accordingly, Alexander is from a different art than Miller et al. and combining the two references would not be obvious. Furthermore, the delay elements of Alexander are disclosed as being possibly buffers or inverters, each of them having a delay unit appropriate to the application of the DLL, such as tens to thousands of picoseconds (col 3., line 47-54). Analog buffers and inverters are fundamentally different than registers, as claimed in claim 8, or other digital delay element capable of storing a data sample. The former cannot store data, therefore they cannot be empty. In consequence, Applicant contends that Alexander does not disclose nor otherwise teaches of reducing the length of the delay chain by bypassing empty registers.

As the Examiner indicates in the Office Action, Miller et al. fail to teach this limitation as well.

With respect to claim 12, Applicant respectfully disagrees with the Examiner's indication that either Miller or Alexander teach of "a timing recovery module for synchronization of the data packet that initiates a transition in the processor".

Claim 13 is a system claim corresponding to method claim 12.

Because neither Miller et al. nor Alexander, taken alone or in combination, teach, suggest or make obvious the invention of Claims 8, 9, 12 or 13, Applicant respectfully submits that Claims 8, 9, 12 and 13, are patentable over these references.

Rejection of Claims 1-7 and 10-11 under 35 U.S.C. § 103(a)

Claims 1, 2 and 10 have been rejected by the Examiner as unpatentable over Alexander in view of Davies (EP 0980186 A2). Claims 3-7 and 11 have been rejected in view of Alexander, Davies and the Applicant's prior art.

The Examiner indicates that Alexander discloses a method of processing samples comprising reading samples into a tapped delay chain, processing samples from taps on the delay chain, subsequent to processing event shifting samples rapidly from the delay chain and reducing the length of the delay chain.

As previously indicated, Applicant respectfully indicates that Alexander does not pertain to processing of data samples, as in amended claim 1, but to the analog processing of clock signals. Alexander does not disclose a tapped delay line able of storing samples, but a delay line made of delay elements that are buffers or inverters, which can only conduct and possible transform (e.g. invert) analog signals. Therefore Applicant contends that Alexander is a reference from a non-analogous art and that in cannot be used in an obviousness rejection.

Applicant further contends that the all of the limitations of amended claim 1 are not found in Davies either nor in the applicant's prior art. Claim 2-7 are dependent on claim 1. Claim 10 is a system claim analogous to Claim 2 and claim 11 is dependent on claim 10. Therefore, because neither Alexander nor Davies nor applicant's prior at, taken alone or in combination, teach, suggest or make obvious the invention of Claims 1-7 and 10- 11, Applicant respectfully submits that Claims 1-7 and 10- 11 are patentable over the cited art.

New claims 15-20 have been added for better describing the invention. These claims are fully supported by the disclosure and recite limitations of claims 1-14 in the same or equivalent language.

CONCLUSION

In view of the above amendments and remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

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